ABSTRACT

A digital phase lock loop circuit including an error generation circuit for generating at least three error signals and a phase error adjustment circuit for generating at least one phase error adjustment signal from the at least three error signals. By using at least three error signals, as opposed to just one, the drift in the sampling phase of the recovered clock is easily detected and corrected to reduce burst errors and to improve loss of lock (LOL) performance.

PH1\846508.7